EXPRESS MAIL LABEL NO. EL863783632US

H418102

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

: Atty. Docket: POU920010166US1

Marvin J. RICH et al.

: APPLICATIONS BRANCH

Serial No. (not yet assigned)

Filed: Herewith

For: VHDL TECHNOLOGY LIBRARY METHOD FOR EFFICIENT CUSTOMIZATION OF CHIP GATE DELAYS

10/038689 10/038689 01/02/02

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D. C. 20231

SIR:

The attached Form PTO-1449 provides a listing of information which may be relevant to the subject application. This IDS is not intended as a representation that better art is not available, nor that the information provided is prior art.

This IDS is submitted under:

XX 37 CFR 1.97(b) - No Fee.

37 CFR 1.97(c) - No Fee, with Certification.

____ 37 CFR 1.97(c) - Fee.

____ 37 CFR 1.97(d) - Fee, Certification & Petition.

The Commissioner is authorized to charge any required fees under 37 CFR 1.17(p) and (i) (1) to Deposit Account No. **09-0463**.

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Bv:

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Jose Gutman / Registration-No. 35,171

Respectfully submitted

FLEIT, KAIN, GIBBONS, GUTMAN & BONGINI P.L.

One Boca Commerce Center 551 NW 77th Street, Suite 111 Boca Raton, Florida 33487-1330

Telephone: (561) 989-9811 Facsimile: (561) 989-9812 Form PTO-1449

U.S. Dept. of Commerce Patent & Trademark Office

List of Documents
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Serial No. (not yet assigned)

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Applicant: Marvin J. RICH et al.

Filing Date: Herewith

Group: (not yet assigned)

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